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(54) **Class AB output amplifier stage.**

(57) An AB class stage is described which comprises two complementary MOSFET final transistors (Qpf, Qnf) connected in a push-pull manner between two supply terminals (+Vcc, -Vcc). In order to attain high linearity, low switching distortion, a high ratio between the maximum output current and the rest current, independence of the rest current from the temperature and manufacturing variables and a circuit simplicity, the circuits determining the rest current and those which provide current to the load are substantially independent of one another. More particularly, two transconductance amplifiers (Tp, Tn) are provided which control the final transistors (Qpf, Qnf) and are dimensioned so as to have zero output current in rest conditions, two voltage generators (Vref(Qpf), Vref(Qnf)) which determine the rest current and two resistors (Rp, Rn) being connected between the gate electrodes of the final transistors and the supply terminals (+Vcc, -Vcc)

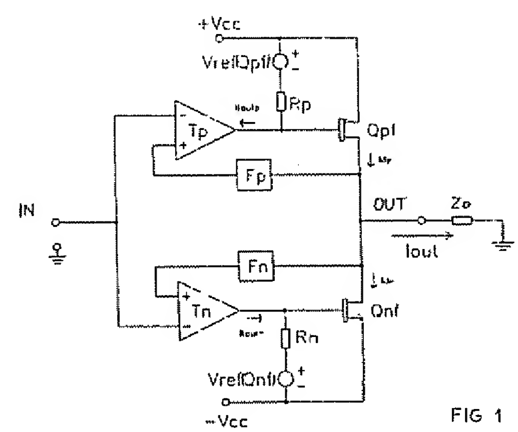


FIG 1

EP 0 684 698 A1

The present invention relates to linear amplifiers and, more particularly, to a class AB output amplifier stage which uses final power components with complementary field effect transistors (MOSFET)

In the planning of the class AB output states, such as those used in operational power amplifiers, it is sought to attain the following characteristics:

- high linearity, that is, low harmonic distortion;
- low distortion owing to the switching between one final power component and the other;
- high ratio between maximum output current and rest current;
- substantial independence of the rest current from the temperature and from variations in the manufacturing parameters if it is produced in an integrated circuit; and
- circuit simplicity

Various class AB output amplifier stages with complementary MOSFET transistors are known which permit one or some of the above characteristics to be attained, but none of them is able to obtain all of them, as would be desirable

The object of the present invention is to propose an output amplifier stage of the type indicated above which has all of these characteristics.

This object is achieved by producing the output amplifier stage generally defined and characterised in the first of the claims following the present description.

The invention and the advantages derived therefrom will become clearer from the following description of some of its embodiments given purely by way of non-limiting example with reference to the appended drawings in which:

- Figure 1 is a basic circuit diagram, partially in block form, of a class AB output stage according to the invention;
- Figure 2 is a basic circuit diagram showing a variant of the diagram of Figure 1; and
- Figures 3, 4 and 5 are circuit diagrams of three embodiments of the output stage in class AB according to the invention.

In Figure 1, two power MOSFET transistors that is, MOS-type field effect transistors, are indicated Qpf and Qnf. They are complementary to one another, more precisely, the first is a p-channel transistor and the second is an n-channel transistor, and are connected in push-pull manner as final components of an AB class output amplifier stage. The drain electrodes of the two transistors are connected to one another and constitute the output terminal, indicated OUT, of the stage and the source electrodes are connected to a first, positive terminal indicated +Vcc and to a second, negative terminal indicated -Vcc of a voltage supply, respectively. The output terminal OUT is connected by means of a load Zo to a reference terminal, represented by the earth symbol, which is at an intermediate potential relative to the potentials of the terminals +Vcc and -Vcc

Two differential-type transconductance amplifiers, designated Tp and Tn, have their respective output terminals connected to the gate electrodes of the transistors Qpf and Qnf respectively, the respective inverting input terminals connected to one another so as to form the input terminal, designated IN, of the stage, and the respective non-inverting input terminals each connected to the output terminal OUT by means of respective feedback systems, indicated Fp and Fn respectively.

Two voltage generators, indicated Vref(Qpf) and Vref(Qnf) are each connected by means of a respective resistor Rp and Rn between the gate electrodes of the transistors, Qpf and Qnf respectively and the supply terminals +Vcc and -Vcc respectively

The transconductance amplifiers Tp and Tn and the feedback systems Fp and Fn are dimensioned such that the output current of the transconductance amplifiers is substantially zero in rest conditions, that is, with the respective inputs at the same voltage. The voltage generators Vref(Qpf) and Vref(Qnf) are dimensioned such that, in the same rest conditions, the voltages between the gate and source electrodes of the transistors, Qpf and Qnp respectively, are such that they cause current of a predetermined value, substantially equal for both transistors, which is the rest current of the stage, to pass. In these conditions, no current is supplied to the load Zo and no current passes through the resistors Rp and Rn

Any change in these conditions, by virtue, for example, of the application of a signal between the input terminal IN and earth, causes an imbalances in both amplifiers Tp and Tn and, therefore, causes the passage of currents Itoutp and Itoutn of opposite signs in the output terminals of both amplifiers and through the resistors connected thereto, Rp and Rn respectively. The voltage drops at the resistors Rp and Rn in turn cause variations of an opposite sign in the voltages Vgs between the gate and source of the final transistors, Qpf and Qnf respectively. Consequently, there are corresponding variations in the conduction of the two transistors and thus variations of opposite signs in the respective drain currents Idp and Idn and the passage of an output current Iout through the load Zo which is equal to the difference between the drain currents of the two transistors.

When dimensioning the circuit, it should be borne in mind that, if Vgsmax(Qpf) and Vgsmax(Qnf) are the voltages between the source and drain of the two transistors enabling the maximum drain currents to be obtained, Itmax(Tp) and Itmax(Tn) are the maximum output currents of the two

transconductance amplifiers, Rp and Rn represent the resistances of the resistors shown with the same reference symbol, and Vref(Qpf) and Vref-(Qnf) represent the voltages of the voltage generators indicated by the same reference symbol, the following conditions should be respected:

$$Itmax(Tp) \cdot Rp + Vref(Qpf) \geq Vgsmax(Qpf) \text{ and}$$
$$Itmax(Tn) \cdot Rn + Vref(Qnf) \geq Vgsmax(Qnf)$$

Furthermore, the amplifiers Tp and Tn should have transconductance values Gmp, Gmn such that the system is stable for a given feedback system and for given characteristics of the final transistors Qpf and Qnf and of the load Zo.

Preferably, the stage is produced symmetrically, that is, with its parts and its components marked p equal and complementary to the parts and components marked n.

It should be used that the feedback systems Fp and Fn, which are used for determining the gain of the stage and for rendering the circuit more stable and more linear, could in some applications be omitted and in their place suitable reference voltage generators could be used for application to the inverting terminals of the amplifiers Tp and Tn. Furthermore, instead of two different feedback systems, a single system could be provided which is common to the two transconductance amplifiers.

An example of a simple common feedback system is shown in Figure 2 where, as a single variant relative to Figure 1, the non-inverting terminals of the amplifiers Tp and Tn are connected to one another and to the intermediate node of a voltage divider, formed by two resistors, indicated Rf1 and Rf2, connected between the output terminal OUT and the earth. The ratio between the resistances of the two resistors determines the gain of the stage.

In the embodiment shown in Figure 3, in which the same reference numerals as used in Figure 2 indicate identical or equivalent elements, the first transconductance amplifier Tp, that is, the one which controls the final p-channel transistor, Qpf, is a differential circuit formed by a pair of n-channel MOSFET transistors arranged with common sources, indicated Qnd1 and Qnd2 and by a first constant current generator Ip connected between the common source electrodes and the supply terminals -Vcc. The drain electrode of the transistor Qnd2 is connected to the supply terminal +Vcc and that of the transistor Qnd1 is the output terminal of the first transconductance amplifier and is therefore connected to the gate electrode of the final transistor Qpf. In an entirely symmetrical manner, the second transconductance amplifier Tn, which is the one controlling the final n-channel transistor, Qnf, is formed by a pair of p-channel MOSFET transistors arranged with common sources, indicated Qpd1 and Qpd2, and by a second constant current generator In connected between the common source electrodes and the feed terminal +Vcc. The drain electrode of the transistor Qpd2 is connected to the supply terminal -Vcc and that of the transistor Qpd1 is the output terminal of the second transconductance amplifier and is therefore connected to the gate electrode of the final transistor Qnf.

The gate electrodes of the transistors Qnd2 and Qpd2 are the non-inverting terminals of the two transconductance amplifiers and are therefore both connected to the feedback system Rf1, Rf2 and the gate electrodes of the transistors Qnd1 and Qpd1 are the inverting terminals of the same amplifiers and are connected to the input terminal IN of the stage.

In this example, the reference voltage generators for determining the rest current of the stage consist, respectively, of the resistor Rp and of the series connection of the transistors Qnd1 and of the constant current generator Ip, as regards the polarisation of the final transistor Qpf, and of the resistor Rn and the series connection of the transistor Qpd1 and of the constant current generator In, as regards the polarisation of the final transistor Qnf. The transconductance amplifiers and the reference voltage generators have components in common such that it is not possible to show them separately as, for example, in Figure 2.

The currents Ip and In of the two constant current generators, indicated by the same reference of the respective generators, should satisfy the following conditions:

$$Ip = N \cdot Vref(Qpf)/Rp \text{ and}$$
$$In = N \cdot Vref(Qnf)/Rn$$

in which N is a number which depends on the dimensional ratio between the transistors of the two differential pairs, and Vref(Qpf) and Vref(Qnf) are the voltages which are to be applied between the gate and source of the final transistors Qpf and Qnf in order to attain the rest current. The dimensional ratio between the transistors, and therefore the number N, is determined by taking account of the maximum gate-source voltage Vgsmax of the final transistors, that is, that which corresponds to the maximum drain current. When considering the upper section of the circuit, if $Vgsmax(Qpf) \leq 2 \cdot Vref(Qpf)$, the transistors Qnd1 and Qnd2 can have equal areas: in fact, in these conditions, at rest, the current Ip is divided into equal parts between Qnd1 and Qnd2, such that $Vref(Qpf) = \frac{1}{2} Ip \cdot Rp$ whilst, with the differential amplifier completely unbalanced, the voltage drop at Rp is $Vgsmax = Ip \cdot Rp$.

If, on the other hand, Vgsmax(Qpf)≥2Vref(Qpf), the area of Qnd1 should be correspondingly smaller than that of Qnd2. For example, if Vref(Qpf)/Rp = 11•Vgsmax(Qpf)/Rp, the area of the transistor Qnd1 should be one tenth of that of Qnd2 and Ip = 11•Vref(Qpf)/Rp. Similar considerations apply for the lower section of the circuit.

In the embodiment of Figure 4, the reference voltage generators Vref(Qpf) and Vref(Qnf) are formed by two MOSFET transistors, one, indicated Qpref, being p-channel and the other, indicated Qnref, being n-channel, with the respective gate and drain electrodes connected together at the two terminals of a constant current generator, indicated Iref, and the respective source electrodes connected respectively to the positive terminal +Vcc and to the negative terminal -Vcc of the voltage supply. The transconductance amplifiers Tp and Tn are differential amplifiers each comprising a pair of MOSFET transistors arranged with common sources. The amplifier Tp comprises two n-channel transistors Q1 and Q2, with the source electrodes connected to the terminal -Vcc by means of a constant current generator Ip' and two p-channel transistors, Q3 and Q4, connected as load elements between the drain electrodes of Q1 and Q2 and the terminal +Vcc and forming a current mirror circuit. As the output terminal of the amplifier Tp, the drain electrode of Q1 is connected to the gate electrode of the transistor Qpf and to a terminal of the resistor Rp. The amplifier Tn is formed in an entirely similar but complementary manner to the amplifier Tp and comprises common source p-channel transistors Q5, Q6, a constant current generator In' and current mirror load n-channel transistors, Q7 and Q8.

In the embodiment of Figure 5, the reference voltage generators Vref(Qpf) and Vref(Qnf) are identical to those described in relation to Figure 4, however, the transconductance amplifiers Tp and Tn are separate and connected to one another. More particularly, the two transconductance amplifiers are formed of a circuit structure of a differential type in which the components cannot be considered as belonging exclusively to one or other amplifier but the operating diagram is still that of Figure 2. The differential structure comprises a first circuit branch comprising two MOSFET transistors Q1 and Q3, the first being n-channel and the second being p-channel, connected by their gate electrodes to the respective drain electrodes, with the source electrodes joined together so as to form an inverting input terminal IN- of the differential circuit and with the drain electrodes connected to the positive terminal +Vcc and to the negative terminal -Vcc of the supply respectively by means of respective constant current generators G1 and G2. The differential structure also comprises a second circuit branch with two MOSFET transistors Q2 and Q4, the first being n-channel and the second being p-channel, with their source electrodes connected together so as to form a non-inverting input terminal IN+ of the differential circuit, their gate electrodes connected to the gate electrodes of the transistors Q1 and Q3 respectively, and their drain electrodes connected respectively to the positive supply terminal +Vcc through a p-channel MOSFET transistor Q5 having the gate electrode connected to the drain electrode and to the negative supply terminal -Vcc via the n-channel MOSFET transistor Q8, connected as the transistor Q5. Two p-channel transistors, Q6 and Q7, and two n-channel transistors, Q9 and Q10, are connected to the transistors Q5 and Q8, respectively, in a current mirror configuration. The drain electrode of the transistor Q6 is connected to the gate electrode of the final n-channel transistor Qnf and the drain electrode of the transistor Q7 is connected to the gate electrode of the final p-channel transistor Qpf. Similarly, the drain electrodes of the transistors Q9 and Q10 are connected to the gate electrodes of Qpf and Qnf respectively. The input terminals of the differential structure, if necessary, are connected to suitable polarisation means, not shown. It should be noted that, in this embodiment, the input signal is applied between the two input terminals IN- and IN+ and that no feedback system is provided between the input and the output of the stage.

The operation of the circuit of Figure 5 will now be considered. At rest, that is, when there is no signal between the input terminals IN- and IN+, a current determined by the two current generators G1 and G2 passes through the transistors Q1 and Q3. The same current which passes through Q1 and Q3 also passes through the transistors Q2 and Q4 if they are dimensionally equal to the respective transistors Q1 and Q3. This same current passes both through the transistor Q5, and is reflected in the transistors Q6 and Q7, and the transistor Q8, and is reflected in the transistors Q9 and Q10. Since the current passing in Q6 is equal to the current passing in Q10, no current passes through the resistor Rn and the voltage at the gate electrode Qnf is the reference voltage determined by the reference voltage generator Vref(Qnf), formed by the transistor Qnref and by the constant current generator Iref. Similarly, since the current passing in Q9 is equal to the current passing in Q7, no current passes through the resistor Rp and the voltage at the gate electrode of Qpf is the reference voltage determined by the reference voltage generator Vref(Qpf), formed by the transistor Qpref and by the constant current generator Iref. Therefore, the same current, that is, the rest current, passes through the final transistors Qpf and Qnf,

and no current passes through the load Zo.

An imbalance of the differential circuit owing to the application of a signal between the two input terminals IN- and IN+, will now be considered, for example in the case in which the potential at the input terminal IN+ is greater than that at the input terminal IN-. This imbalance causes an increase in the current in Q4 and a reduction of the current in Q2 and, therefore, an increase in the currents in Q8, Q9 and Q10 and a reduction of the currents in Q5, Q6 and Q7. Owing to the different currents in Q6 and in Q10 and of the different currents in Q9 and Q7, respective different currents will pass in the resistors Rn and Rp, such that the voltage between the gate and source electrodes of the transistor Qpf, Vgs(Qpf), increases relative to the reference voltage Vref(Qpf) and that of Qnf decreases relative to the reference voltage Vref(Qnf). Therefore, the currents passing through the two final transistors are also different, such that a current, which is the difference between the currents of the two final transistors, passes through the load Zo.

From a practical analysis of the different embodiments described above, it is noted that the output amplifier stage according to the invention has high linearity and low distortion when switching between one final transistor and the other since there is no discontinuity in the command of the final transistors and since the circuits determining the rest current and the circuits supplying the required current to the load function substantially independently of one another. This further enables a high ratio to be obtained between the maximum output current and the rest current, since the rest current can be set with great precision at very low values and the dynamics of the final components are not limited at all by the control circuit. The dependence on the temperature and on the variations in the parameters of the process can also be limited to a great extent by virtue of the possibility of compensation deriving from the total symmetry of the control circuits of the two complementary final components. Finally, the simplicity of the circuit is evident and therefore the stage according to the invention lends itself to production in integrated circuits with very restricted areas.

Although only some embodiments of the invention have been illustrated and described, it is evident that numerous variations and modifications are possible within the scope of the same inventive concept. For example, the transconductance amplifiers could be produced with bipolar transistors instead of with MOSFET transistors and the resistors Rp and Rn could be resistive means having substantially the structure of MOSFET transistors with the drain and gate electrodes short-circuited; furthermore, two power components each comprising more than one transistor could be provided in the place of the MOSFET power transistors Qpf and Qnf.

Claims

1. A class AB output amplifier stage comprising a first and a second field effect transistor power component (Qpf, Qnf) which are complementary to one another, each having a first and a second power electrode and a control electrode, and being connected, in push-pull manner relative to one another, by the respective first power electrodes to a first (+Vcc) and to a second (-Vcc) terminal of a voltage supply respectively, and the second power electrodes connected to one another and to an output terminal of the stage (OUT), characterised in that it comprises:
   - a first (Tp) and a second (Tn) transconductance amplifier each having an output terminal connected to the control electrode of the first (Qps) and of the second (Qnf) power component respectively and an input terminal connected to the input terminal of the other transconductance amplifier, so as to form an input terminal (IN) of the stage, and being dimensioned so as to have an output current which is substantially zero in rest conditions;
   - a first (Vref(Qpf)) and a second (Vref(Qnf)) voltage generator connected to the control electrode of the first (Qpf) and of the second (Qnf) power component respectively, the voltages of these generators being selected so as to determine currents which are substantially equal through the first and second power components in rest conditions of the stage; and
   - a first (Rp) and a second (Rn) resistive means connected between the control electrode of the first (Qpf) and of the second (Qnf) power component respectively and the first (+Vcc) and the second (-Vcc) terminal of the voltage supply respectively.

2. A stage according to Claim 1, in which each of the transconductance amplifiers (Tp, Tn) comprises an inverting input terminal which is the above input terminal connected to the input terminal (IN) of the stage and a non-inverting input terminal, and in which the non-inverting input terminal of each of the transconductance amplifiers (Tp, Tn) is connected to a respective reference voltage generator.

3. A stage according to Claim 2, in which the reference voltage generators consist of respective feedback systems (Fp, Fn) connected to the output terminal (OUT) of the stage.

4. A stage according to Claim 2, in which the reference voltage generators consist of a common feedback system (RF1, RF2) connected to the output terminal (OUT) of the stage.

5. A stage according to Claim 4, in which a reference terminal is provided which is common to the input and to the output of the stage, and in which:
   - the first and the second power components consist of a first (Qpf) and of a second (Qnf) field effect power transistor being p-channel and n-channel respectively, the first and the second power electrode being the source and drain electrodes respectively and the control electrode being the gate electrode;
   - the first transconductance amplifier (Tp) comprises a first pair of n-channel field effect transistors (Qnd1, Qnd2) in common source arrangement and a first current generator (Ip) connected between the common source electrodes and the second supply voltage terminal (-Vcc), the drain of one (Qnd2) of the transistors of the first pair being connected to the first supply terminal (+Vcc) and the drain of the other transistor (Qnd1) of the first pair being the output terminal of the first transconductance amplifier (Tp);
   - the second transconductance amplifier (Tn) comprises a second pair of p-channel field effect transistors (Qpd1, Qpd2) in the common source arrangement and a second current generator (In) connected between the common source electrodes and the first supply terminal (+Vcc), the drain of one (Qpd2) of the transistors of the second pair being connected to the second supply terminal (-Vcc) and the drain of the other (Qpd1) of the transistors of the second pair being the output terminal of the second transconductance amplifier (Tn), the gate electrodes of the transistors of the first and of the second pair being connected to one another in pairs, so as to form the above inverting terminal, which is the input terminal (IN) of the stage, and the said non-inverting terminal;
   - the first resistive means is a first resistor (Rp) connected directly between the gate electrode of the first power transistor (Qpf) and the first supply terminal (+Vcc) and the first current generator (Ip) constitutes, together with the first resistor (Rp), the first reference voltage generator (Vref(Qpf));
   - the second resistive means is a second resistor (Rn) directly connected between the gate electrode of the second power transistor (Qnf) and the second supply terminal (-Vcc) and the second current generator (In) constitutes, together with the second resistor (Rn), the second reference voltage generator (Vref(Qnf)); and
   - the feedback system comprises a voltage divider (Rf1, Rf2) connected between the output terminal (OUT) of the stage and the common reference terminal and having the intermediate node connected to the common gate electrodes of the transistors (Qnd2, Qpd2) of the two transconductance amplifiers which constitute the non-inverting terminal

6. A stage according to Claim 4, in which:
   - the first resistive means is a first resistor (Rp) connected to the first supply terminal (+Vcc) via a first p-channel field effect reference transistor (Qpref) having common drain and gate electrodes and the second resistive means is a second resistor (Rn) connected to the second supply terminal (-Vcc) via a second n-channel field effect reference transistor (Qnref) having common drain and gate electrodes, a reference current generator (Iref) being connected between the common gate and drain electrodes of the first reference transistor and the common gate and drain electrodes of the second reference transistor, so as to form the first and the second voltage generators (Vref(Qpf), Vref(Qnf)) together with the first and second reference transistors (Qpref, Qnref)

7. A stage according to Claim 6, in which the first and the second transconductance amplifiers (Tp, Tn) comprise a first and a second differential amplifier.

8. A stage according to Claim 7, in which:
   - the first differential amplifier (Tp) comprises a first pair of n-channel field effect transistors (Q1, Q2) in the common source configuration, a constant current generator (Ip) connected between the common source electrodes and the sec-

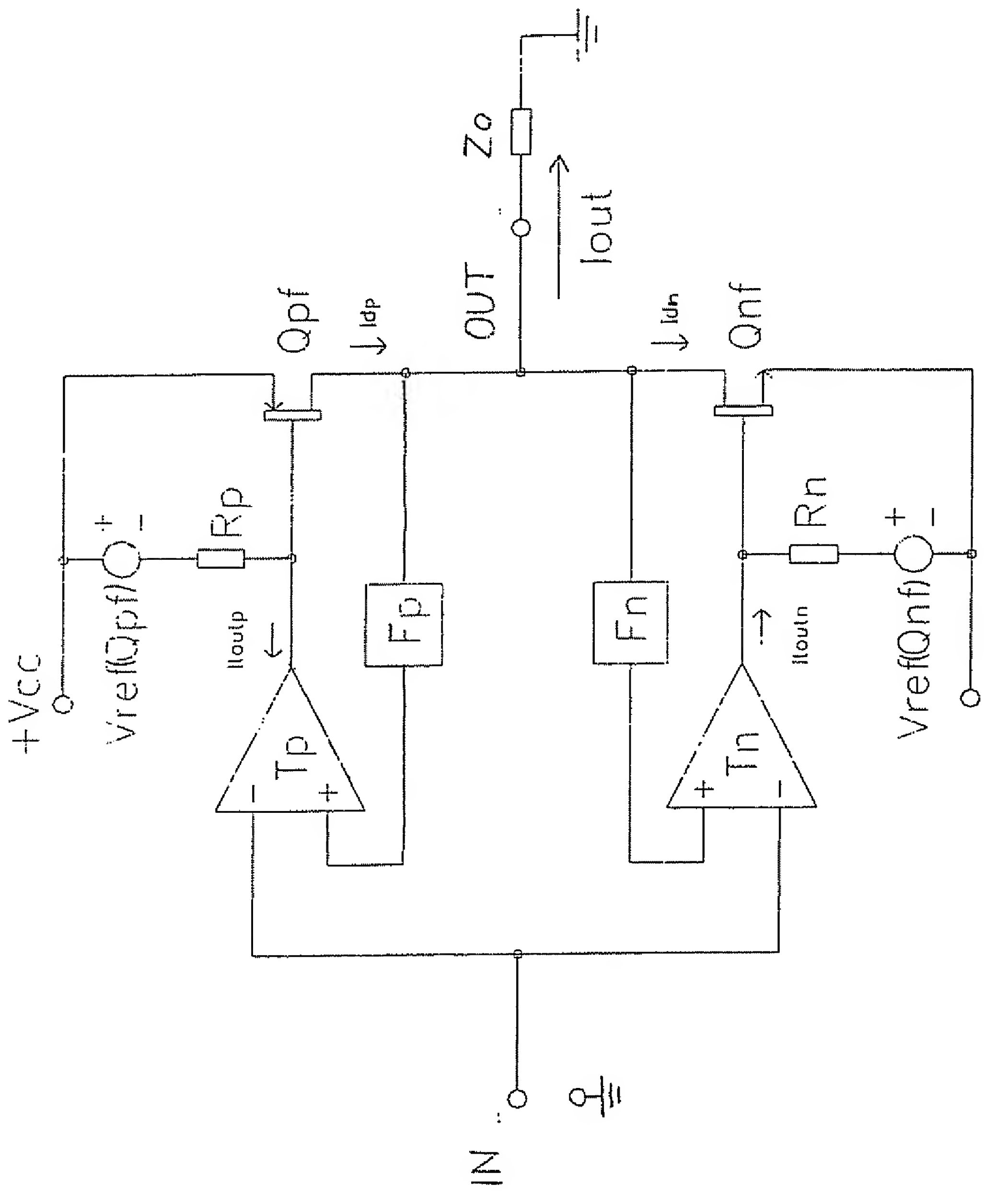
ond supply terminal (-Vcc) and a second pair of p-channel field effect transistors (Q3, Q4) connected as load elements between the drain electrodes of the transistors of the first pair (Q1, Q2) and the first supply terminal (+Vcc) and connected between each other in the current mirror configuration; and

- the second differential amplifier (Tn) comprises a third pair of p-channel field effect transistors (Q5, Q6) in the common source configuration, a constant current generator (In) connected between the common source electrodes and the first supply terminal (+Vcc) and a fourth pair of n-channel field effect transistors (Q7, Q8) connected as load elements between the drain electrodes of the transistors of the third pair (Q5, Q6) and the second supply terminal (-Vcc) and connected to one another in the current mirror configuration.

9. A stage according to Claim 1, in which the first resistive means is a first resistor (Rp) connected to the first supply terminal (+Vcc) via a first p-channel field effect transistor (Qpref) having common drain and gate electrodes and the second resistive means is a second resistor (Rn) connected to the second supply terminal (-Vcc) via a second n-channel field effect reference transistor (Qnref) having common drain and gate electrodes, a reference current generator (Iref) being connected between the common drain and gate electrodes of the first reference transistor and the common drain and gate electrodes of the second reference transistor, so as to form the first and second voltage generators (Vref(Qpf), Vref(Qnf)) together with the first and second reference transistors (Qpref, Qnref).

10. A stage according to Claim 9, in which the first and the second transconductance amplifiers (Tp, Tn) are formed in a differential structure comprising:

- a first circuit branch inserted between the first (+Vcc) and the second (-Vcc) supply terminals and comprising, in series relative to each other, a first constant current generator (G1) with a terminal connected to the first (+Vcc) supply terminal, a first n-channel field effect transistor (Q1) with the drain electrode connected to the gate electrode, a second p-channel field effect transistor (Q3) with the drain electrode connected to the gate electrode, and a second constant current generator (G2) with a terminal connected to the second supply terminal (-Vcc), the source electrodes of the first (Q1) and second (Q3) transistors being connected to one another so as to form the inverting input terminal of the differential structure which constitutes the said input terminal (IN) of the stage;
- a second circuit branch comprising a third and a fourth field effect transistors (Q2, Q4), the first being n-channel and the second being p-channel, with their source electrodes connected together so as to form a non-inverting input terminal (IN+) of the differential structure which constitutes a further input terminal of the stage, with the respective gate electrodes connected to the gate electrodes of the first (Q1) and of the second (Q3) field effect transistors of the first branch respectively and with the respective drain electrodes connected to the common drain and source electrodes of a fifth and a sixth field effect transistor, respectively, p-channel (Q5) and n-channel (Q8) having respective source terminals connected to the first (+Vcc) and to the second (-Vcc) supply terminal respectively;
- a first pair of p-channel field effect transistors (Q6, Q7) having the gate electrodes connected to the gate electrodes of the fifth field effect transistor (Q5), the source electrodes connected to the first supply terminal (+Vcc) and the drain electrodes connected one to the control electrode of the second power component (Qnf) and the other to the control electrode of the first power component (Qpf); and
- a second pair of n-channel field effect transistors (Q9, Q10) having the gate electrodes connected to the gate electrode of the sixth (Q8) field effect transistor, the source electrodes connected to the second supply terminal (-Vcc) and the drain electrodes connected one to the control electrode of the first power component (Qpf) and the other to the control electrode of the second power component (Qnf).


+Vcc
Vref(Qpf)
Rp
Illoutp
Tp
Fp
Qpf
Idp
OUT
Iout
Zo
Fn
Idn
Qnf
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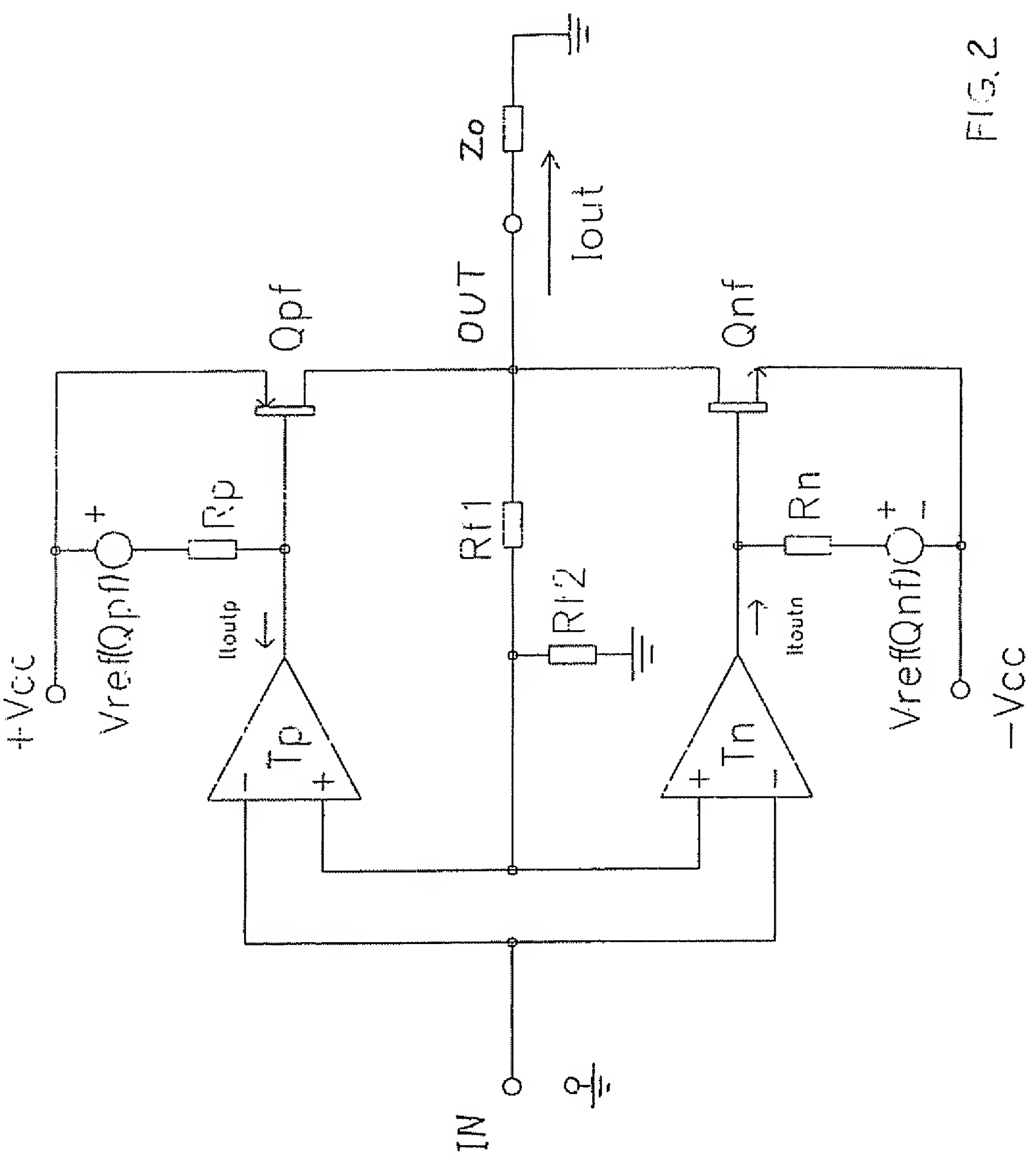
Iloutn
Tn
Vref(Qnf)
-Vcc
IN

FIG. 1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Rf1
Rf2
IN
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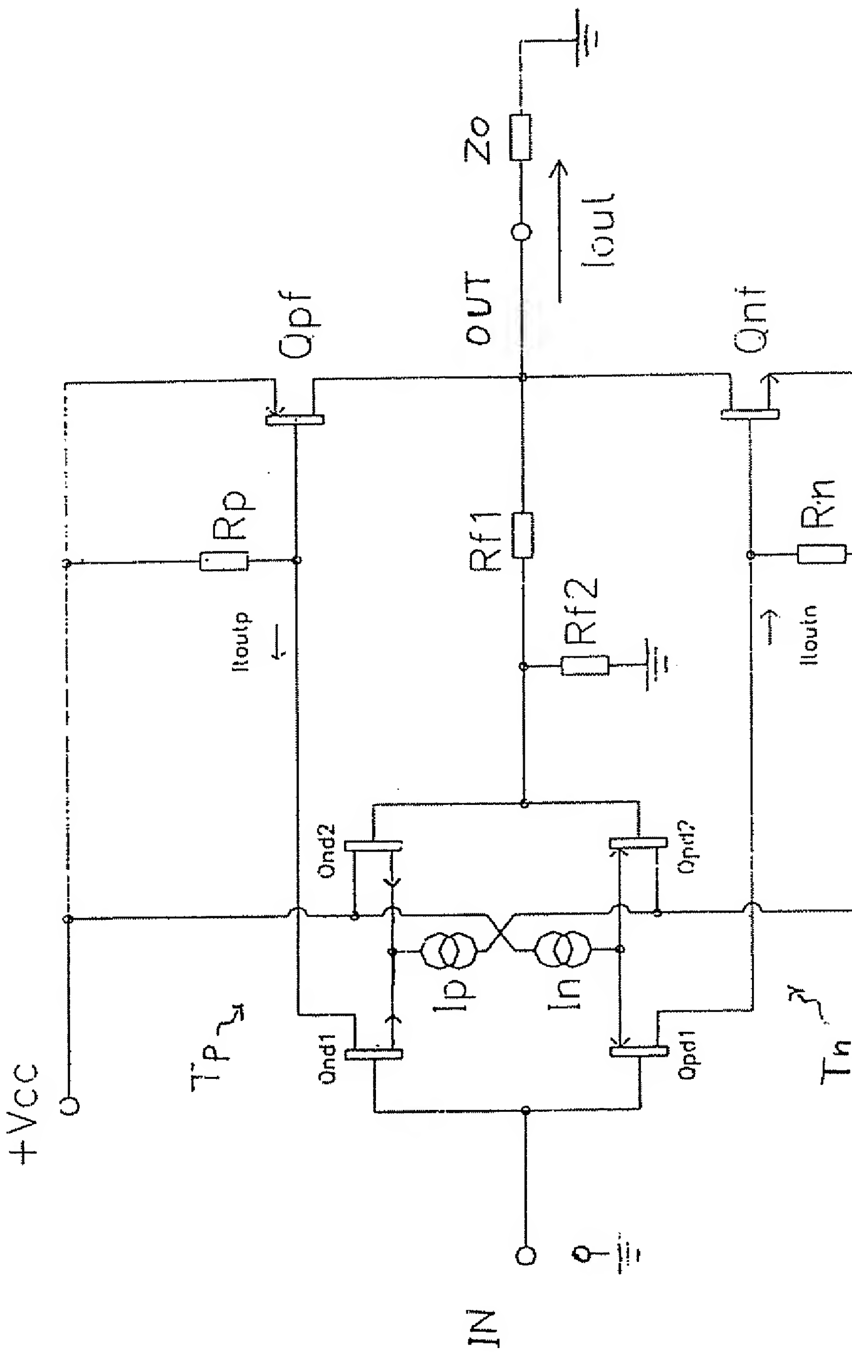
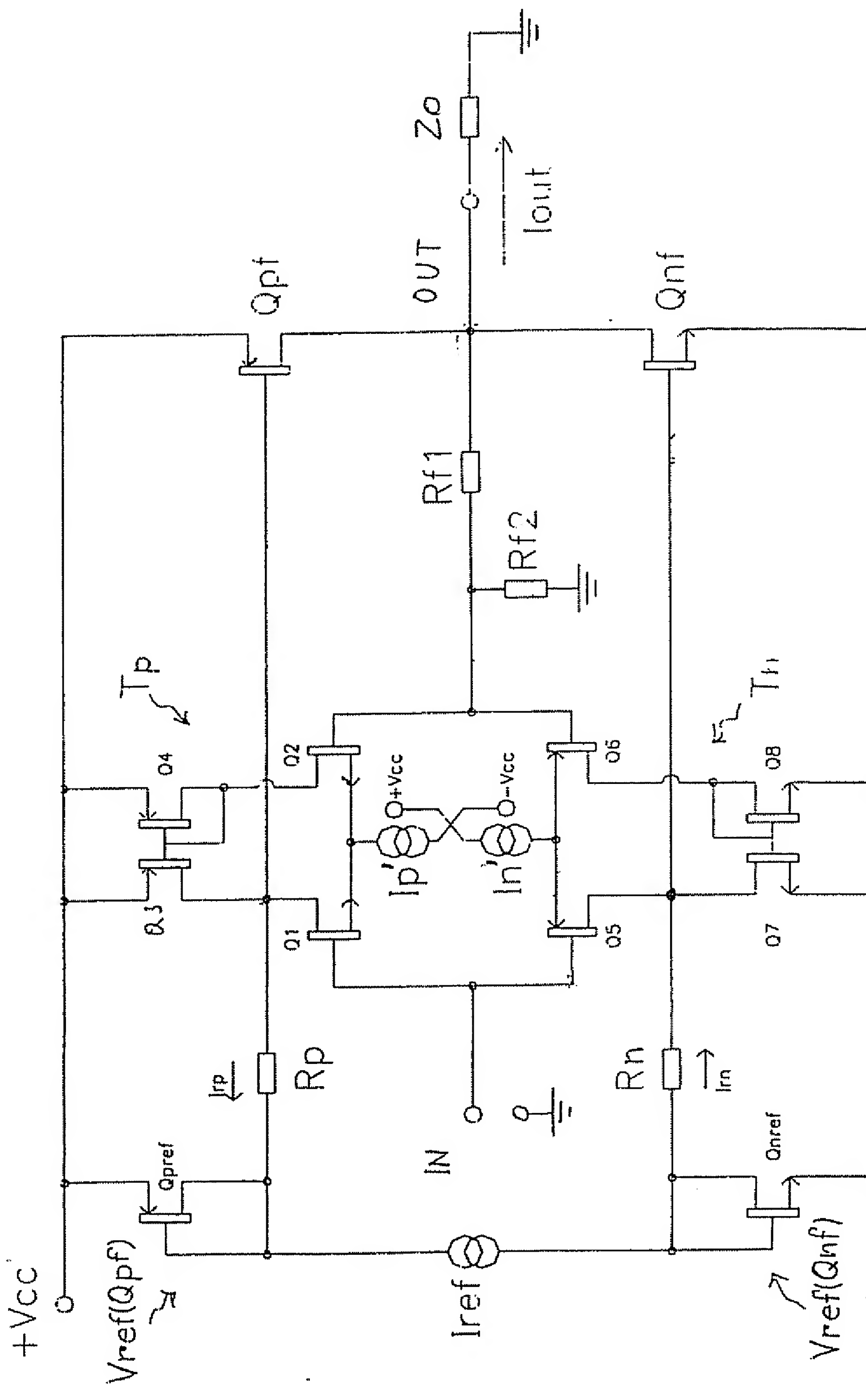
Tn
Vref(Qnf)
-Vcc

FIG. 2



+Vcc
-Vcc
Tp
Tn
Qnd1
Qnd2
Qpd1
Qpd2
Ip
In
IN
OUT
Zo
Iout
Qpf
Qnf
Rp
Rn
Rf1
Rf2
Itoutp
Itoutn

FIG. 3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Qpref
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Rp
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Q4
Tp
Q1
Q2
Qpf
Iref
IN
Ip'
In'
+Vcc
-Vcc
Rf1
Rf2
OUT
Iout
Zo
Q5
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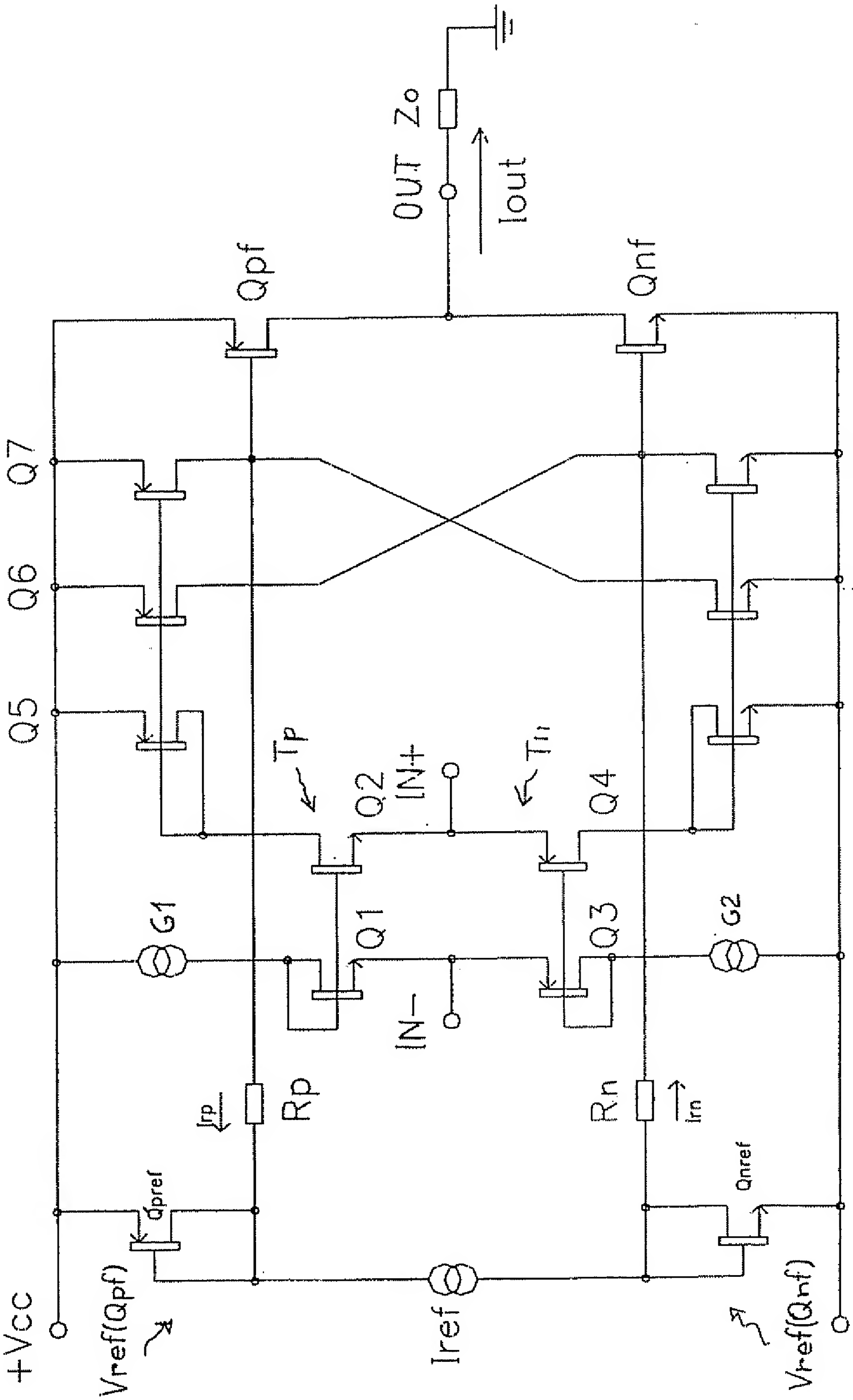
Rn
Irn
Qnref
Vref(Qnf)
-Vcc
Q7
Q8
Tn
Qnf

FIG. 4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IN−
G1
Q1
Q2
IN+
Tp
Q5
Q6
Q7
Qpf
OUT
Zo
Iout
Qnf
Q10
Q9
Q8
Tn
Q4
Q3
G2
Rn
Irn
Qnref
Vref(Qnf)
−Vcc

FIG.5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0239

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 535 951 (NEC CORP.) * abstract; figure 2 * ---	1	H03F1/00 H03F3/30
A	US-A-4 866 398 (GULCZYNSKI) * abstract; figure 4 * ---	2	
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 99 (E-594) 31 March 1988 & JP-A-62 230 206 (TOSHIBA CORP.) 8 October 1987 * abstract * ---	1,7,8	
A	US-A-5 039 953 (SU) * abstract; figure 2 * -----	10	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	14 October 1994	Danielidis, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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